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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/059,987	01/29/2002	Steven Tinsley	TI-33936	6817

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EXAMINER
TRAN, ANH Q

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/059,987	TINSLEY ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-18 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-18 of copending Application No. 10/008,039. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the features of the claimed invention are the same.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

4. Claims 1, 3-7, 9, 11-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Gabara et al (6,107,882).

Regarding claim 1, Gabara shows a driver circuit (710, Fig, 8A) for driving a load (910, Fig. 9) with a differential signal (Vout- and Vout+), comprising:

A first output drive portion (MP1 & MP2) operably coupled to a power supply rail (Vdd); a second output drive portion (MN1, MN2, MP2, MP4) coupled to the first output drive portion, a low voltage differential input signal (Vin- and Vin+), and further comprising output terminals (Vout- and Vout+) coupled to the load, and operably coupled with a current source (MN3), wherein the second output drive portion is operable to switch alternate polarity terminals of the load to the current source; and

A common mode compensation circuit (720) coupled to the output terminals of the second output drive portion and the first output drive portion, wherein the common mode compensation circuit is operable to detect a common mode voltage associated with the load and generate a compensation signal in response thereto, wherein the first output drive portion is operable to vary an impedance associated therewith in response to the compensation signal, thereby regulating a common mode voltage associated with the load, whereby the differential signal is transmitted to the load at a high rate of speed with a high compliance of the common mode output even at high current loading conditions, while maintaining a simple pre-driver circuit with a wide common mode range (CMVR, col. 2, lines 64-65).

Regarding claim 3, Gabara shows the power supply rail is positive voltage (Vdd).

Regarding claims 4-6, Gabara shows the two switching MOS transistors (MN1, MP2 and MN2, MP4) and the current source (MN3) coupled to Vss.

Regarding claim 7, Gabara shows the common mode compensation circuit comprises:

A common mode voltage monitor circuit operable to provide the common mode voltage associated with a node (815) of a voltage divider (R1 & R2) coupled across the output terminals for the load; and

A common mode error amplifier circuit (810) operable to receive a reference voltage input (Vref) and the common mode voltage from the common mode voltage monitor circuit, and generate a compensation signal (820) to the first output drive portion in response thereto, whereby the impedance of the first output drive portion is adjusted such that voltage regulation of the common mode dc voltage is provided.

Regarding claim 11, Gabara discloses the driver are compatible with LVDS or CML load.

The limitations of claims 12-17 are rejected as above claims.

The apparatus described above is applicable to the method claim 18.

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1-2, 7, 8, & 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Tinsley et al (6,369,621).

Regarding claim 1, Tinsley shows a driver circuit (30, Fig. 3) for driving a load (RL) with a differential signal, comprising:

A first output drive portion (Q3-Q4) operably coupled to a power supply rail (Vcc); a second output drive portion (Q1-Q2) coupled to the first output drive portion, a low voltage differential input signal (in1 and in2), and further comprising output terminals coupled to the load, and operably coupled with a current source (Iref), wherein the second output drive portion is operable to switch alternate polarity terminals of the load to the current source; and

A common mode compensation circuit (A2) coupled to the output terminals of the second output drive portion and the first output drive portion, wherein the common mode compensation circuit is operable to detect a common mode voltage associated with the load and generate a compensation signal in response thereto, wherein the first output drive portion is operable to vary an impedance associated therewith in response to the compensation signal, thereby regulating a common mode voltage associated with the load, whereby the differential signal is transmitted to the load at a high rate of speed with a high compliance of the common mode output even at high current loading conditions, while maintaining a simple pre-driver circuit with a wide common mode range.

Regarding claim 1, Tinsley shows the transistors are bipolar transistor.

Regarding claim 7, Tinsley shows the common mode compensation circuit comprises:

A common mode voltage monitor circuit operable to provide the common mode voltage associated with a node of a voltage divider (R1 & R2) coupled across the output terminals for the load; and

A common mode error amplifier circuit (A2) operable to receive a reference voltage input (Vref) and the common mode voltage from the common mode voltage monitor circuit, and generate a compensation signal (output from A2) to the first output drive portion in response thereto, whereby the impedance of the first output drive portion is adjusted such that voltage regulation of the common mode dc voltage is provided.

Regarding claim 8, Tinsley shows the resistors have the same value.

Regarding claim 10, Tinsley shows the reference voltage circuit generates a reference voltage of about 1.2 volts (col. 2, line 19).

The limitations of claim 12 are rejected above claims.

The apparatus described above is applicable to the limitations of the method claim 18.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

7. Van Brunt et al (5,592,510) discloses the common mode driver for wide range of common mode voltage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 703-306-4507. The examiner can normally be reached on M-TH (7:00-5:30) Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7724 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Anh Tran
September 10, 2002